Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A high-voltage input tolerant receiver adapted to receive an external signal varying between a ground potential and a defined voltage limit for the receiver, the receiver being designed to output an internal signal varying between the ground potential and a voltage less than the defined voltage limit for the receiver, comprising:

a pad which receives the external signal;

a control circuit that receives the external signal input from the pad and outputs a first control signal and a second control signal when the external signal is higher than a first voltage;

a first clamp circuit that receives the external signal input from the pad, outputs an intermediate signal equivalent to the external signal, and clamps the intermediate signal to a second voltage lower than the first voltage in response to receiving the first control signal;

a level keeper circuit that pulls the intermediate signal up to a third voltage less than or equal to the first voltage in response to receiving the second control signal; and

a buffer circuit that receives the intermediate signal and

outputs the internal signal.

[c2] 2. A high-voltage input tolerant receiver according to claim 1, wherein the first clamp circuit includes:
a first n-channel transistor receiving the external signal and having a gate coupled to the third voltage, and
a first p-channel transistor connected in parallel with the first n-channel transistor and having a gate coupled to the first control signal.

[c3] 3. A high-voltage input tolerant receiver according to claim 1, wherein
the buffer circuit includes a plurality of inverters coupled in series to receive and propagate the intermediate signal,
the level keeper circuit includes a second p-channel transistor with a source coupled to the third voltage and a gate to receive the second control signal, and
a third p-channel transistor connected between the drain of the second p-channel transistor and the output node of said first clamp circuit and having a gate to receive output signals from the plurality of inverters.

[c4] 4. A high-voltage input tolerant receiver according to claim 1, wherein the control circuit includes:
a switch that outputs the first control signal equivalent to the external signal when the external signal is higher

than the first voltage,
a second clamp circuit that clamps the first control signal to a voltage lower than the first voltage in response to receiving the first control signal, and
a differential amplifier circuit that receives the clamped first control signal and outputs the second control signal.

[c5] 5. A high-voltage input tolerant receiver according to claim 4, wherein the switch includes a fourth p-channel transistor having a source to receive the external signal, the fourth p-channel transistor being turned on when the external signal is higher than the first voltage.

[c6] 6. A high-voltage input tolerant receiver according to claim 4 or 5, wherein said second clamp means includes a second n-channel transistor receiving the first control signal and having a gate to receive the third electric potential.

[c7] 7. A method of reducing distortion of analog signals in a high voltage input tolerant receiver, the method comprising:
providing a pad to receive an external signal input;
providing a control circuit that receives the external signal input from the pad and outputs a first control signal and a second control signal when the external

signal is higher than a first voltage;

providing a first clamp circuit to receive the external signal input from the pad, outputs an intermediate signal equivalent to the external signal, and clamps the intermediate signal to a second voltage lower than the first voltage in response to receiving the first control signal;

providing a level keeper circuit to pull the intermediate signal up to a third voltage less than or equal to the first voltage in response to receiving the second control signal; and

providing a buffer circuit to receive the intermediate signal and outputs the internal signal.

[c8] 8. The method according to claim 7, wherein the method includes:

disabling the output of the first control signal and the second control signal when the external signal is lower than the first voltage;

disabling the level keeper circuit when the external signal is equal to or lower than the first voltage; and

enabling the first clamp circuit to output the external signal from the pad as the intermediate signal.

[c9] 9. The method according to claim 7, wherein power dissipation of the high-voltage input tolerant receiver is reduced by fixing the intermediate signal at a defined in-

put/output standard voltage when an input voltage to the receiver exceeds a specified input voltage limit for the receiver and enabling the level keeper circuit only when an input voltage exceeds the specified input voltage limit for the receiver.